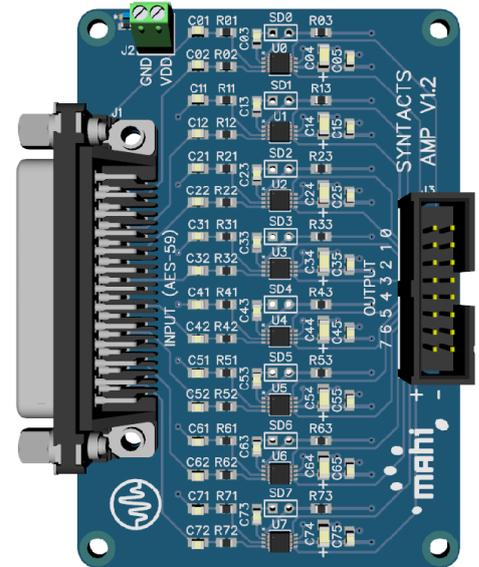




# Class AB Vibrotactor Signal Amplifier

## 1 Overview

- Class AB linear power amplification (2 V/V, 1W max per channel)
- 8-channel vibrotactor I/O
- Standard AES59-2012 input
- IDC output allows connection to range of devices



## 2 Description

- This amplifier uses the Texas Instruments TPA6211A1 3.1W fully differential audio power amplifier. This linear power amplifier simplifies the integration of pieces of complex systems through its analog nature.
- The linear power amplification also means that the signal sent to the output is the actual waveform from the signal generator as opposed to Class D amplifiers that output PWM versions of the input.
- Input is designed to the Audio Engineering Society (AES) 59-2012 standard to quickly interface with audio equipment. It is also a standard D-Sub DB25 connector so that users can create a custom connector to their own signal generation hardware.
- Output is a 16-pin IDC compatible header, great for ribbon cables in final assembly or jumper cables in prototyping stages.
- Sizing of surface mount components allows human assembly, to keep production cost low
- Gain is adjustable based on selection of resistors
- Blue LED power indicator built into board

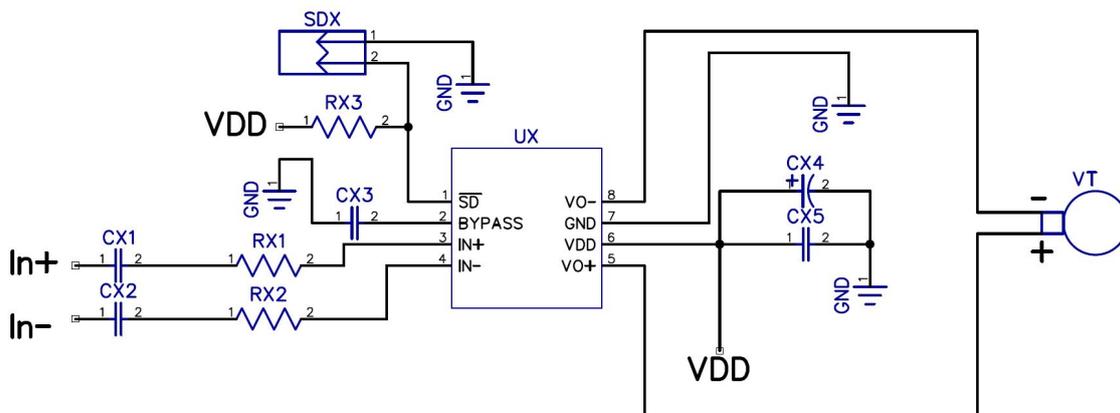
### 3 Technical specification

	Unit	Value
Recommended supply voltage	V	2.5 - 5.5
Absolute supply voltage limits	V	-0.3 - 6.0
Board dimensions	<i>in * in * in</i>	3.5*2.375*0.54
n° of channels	--	8
Signal input voltage range	V	±5

Table 1: Technical Specifications for amplifier board

### 4 Component Values

Components are arranged on the board such that all the parts of each channel are near each other. The labeling of the components is done to simplify identification of the component. For example, the label "C41" means it is "C1" associated with channel 4. The schematic for a single channel is included in Fig.4 as well as a materials list for a single amplifier channel in Table2.



Component	Description	Digi-Key P/N
CX1, CX2, CX3, CX5	0.22µF	1276-1284-1-ND
CX4	10µF	478-8540-1-ND
RX1, RX2	20kΩ	P20KDACT-ND
RX3	100kΩ	P100KDACT-ND
UX	TPA6211A1	296-29059-1-ND
Output Header	16 pos, vertical	SAM10835-ND
Input D-SUB	DB25 female sockets	H122879-ND

Table 2: Component values and description

## 5 Gain Selection

This board is designed with a amplitude gain of 2V/V in order to accommodate input from professional audio equipment. Certain uses may require different gain values to use the full output potential of the board. The amplifiers can output signals roughly up to  $\pm V_{DD}$ . Depending on the function generator and the tactors, the user may need a different gain value. The equation to calculate gain is

$$Gain = \frac{V_o}{V_i} = \frac{R_f}{R_i}$$

The value of each internal feedback resistor ( $R_f$ ) are trimmed to 40k $\Omega$ , and  $R_i$  is represented in Fig. 4 as  $R1 - X$  and  $R2 - X$ . To construct the proper output signal both the positive and negative input channels should have the same gain.

## 6 Board Measurements

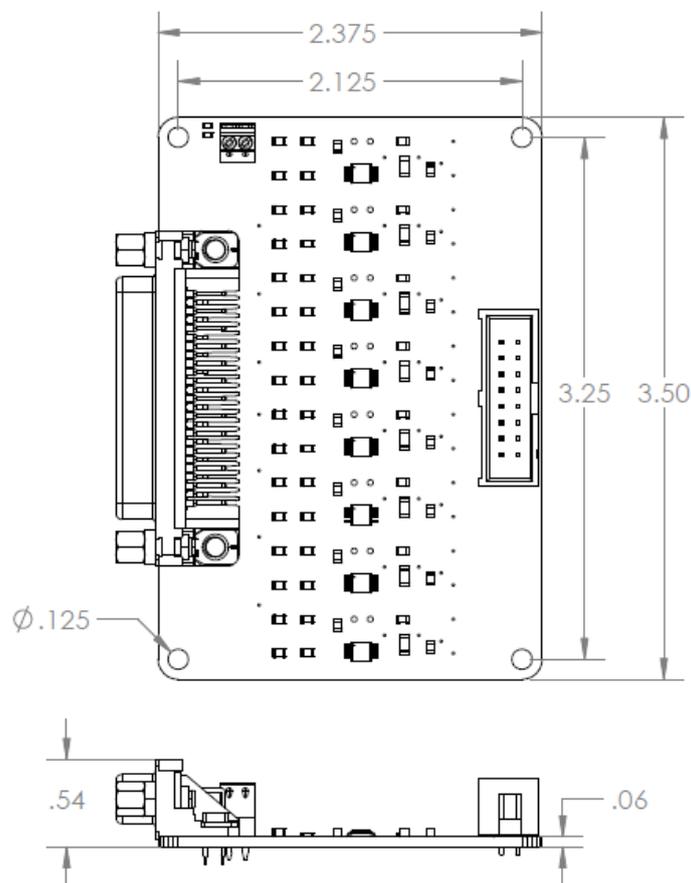


Figure 1: Board Major Dimensions (inches)

# 7 Amplifier Chip Datasheet



TPA6211A1-Q1

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## TPA6211A1-Q1 3.1-W Mono Fully Differential Audio Power Amplifier

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- 3.1 W Into 3 Ω From a 5-V Supply at THD = 10% (Typical)
- Low Supply Current: 4 mA (Typical) at 5 V
- Shutdown Current: 0.01 μA (Typical)
- Fast Startup With Minimal Pop
- Only Three External Components
  - Improved PSRR (–80 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation
  - Fully Differential Design Reduces RF Rectification
  - –63-dB CMRR Eliminates Two Input Coupling Capacitors

### 2 Applications

- Automotive Audio
- Emergency Calls
- Driver Notifications
- Cluster Chimes

### 3 Description

The TPA6211A1-Q1 device is a 3.1-W mono fully-differential amplifier designed to drive a speaker with at least 3-Ω impedance while consuming only 20-mm<sup>2</sup> total printed-circuit board (PCB) area in most applications. The device operates from 2.5 V to 5.5 V, drawing only 4 mA of quiescent supply current. The TPA6211A1-Q1 device is available in the space-saving 8-pin MSOP (DGN) PowerPAD™ package.

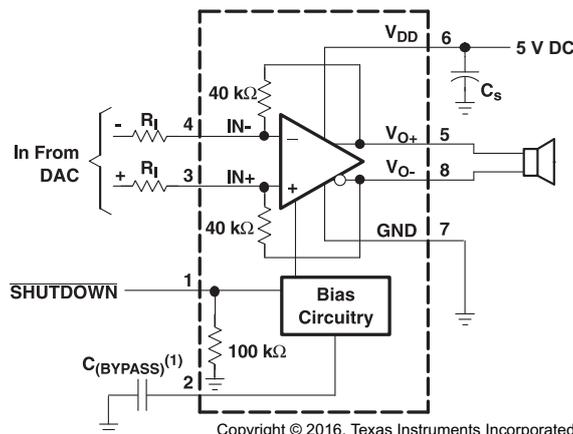
The device includes features such as a –80-dB supply voltage rejection from 20 Hz to 2 kHz, improved RF-rectification immunity, small PCB area, and a fast start-up with minimal pop makes the TPA6211A1-Q1 device ideal for emergency call applications. Additionally, the device supports low-power needs in infotainment and cluster applications, such as cluster chimes or driver notification.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6211A1-Q1	MSOP-PowerPAD (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Application Circuit



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(1) C<sub>(BYPASS)</sub> is optional



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**4 Revision History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (January 2014) to Revision C</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> </ul>	<b>1</b>
<ul style="list-style-type: none"> <li>Added missing Max Ambient Temperature values to <a href="#">Table 2</a>.....</li> </ul>	<b>14</b>
<ul style="list-style-type: none"> <li>Changed 45.9 to 71.7, 1.27 to 1.25, and 91.7 to 60 in <a href="#">Equation 12</a> .....</li> </ul>	<b>15</b>

<b>Changes from Revision A (November 2013) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added three new equations to the <i>DIFFERENTIAL OUTPUT VERSUS SINGLE-ENDED OUTPUT</i> section in order to show difference between single-ended and differential output .....</li> </ul>	<b>15</b>

<b>Changes from Original (June 2011) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Deleted <i>Designed for Wireless or Cellular Handsets and PDAs</i> from <i>Features</i> list.....</li> </ul>	<b>1</b>
<ul style="list-style-type: none"> <li>Deleted <i>Ordering Information</i> table .....</li> </ul>	<b>3</b>
<ul style="list-style-type: none"> <li>Changed reference from "equation 6" to <a href="#">Equation 25</a> in the <i>High-Pass Filter</i> section.....</li> </ul>	<b>20</b>

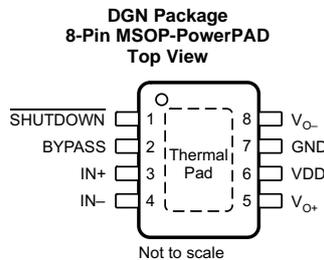


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**5 Pin Configuration and Functions**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
BYPASS	2	I	Mid-supply voltage, adding a bypass capacitor improves PSRR
GND	7	I	High-current ground
IN-	4	I	Negative differential input
IN+	3	I	Positive differential input
SHUTDOWN	1	I	Shutdown pin (active low logic)
Thermal Pad	—	—	Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.
V <sub>DD</sub>	6	I	Power supply
V <sub>O+</sub>	5	O	Positive BTL output
V <sub>O-</sub>	8	O	Negative BTL output

**6 Specifications**

**6.1 Absolute Maximum Ratings**

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, V <sub>DD</sub>	-0.3	6	V
Input voltage, V <sub>I</sub>	-0.3	V <sub>DD</sub> + 0.3 V	V
Continuous total power dissipation	See <a href="#">Dissipation Ratings</a>		
Lead temperature 1.6 mm (1/16 Inch) from case for 10 s	DGN		260 °C
Operating free-air temperature, T <sub>A</sub>	-40	105	°C
Junction temperature, T <sub>J</sub>	-40	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**6.2 ESD Ratings**

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



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**6.3 Recommended Operating Conditions**

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage	2.5	5.5	V
V <sub>IH</sub>	High-level input voltage	SHUTDOWN		V
V <sub>IL</sub>	Low-level input voltage	SHUTDOWN		V
T <sub>A</sub>	Operating free-air temperature	-40	105	°C

**6.4 Thermal Information**

THERMAL METRIC <sup>(1)</sup>	TPA6211A1-Q1		UNIT
	DGN (MSOP-PowerPAD)		
	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	71.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	55.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	44.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	44.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	19.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

**6.5 Electrical Characteristics**

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OS</sub>	Output offset voltage (measured differentially) V <sub>I</sub> = 0-V differential, Gain = 1 V/V, V <sub>DD</sub> = 5.5 V	-9	0.3	9	mV
PSRR	Power supply rejection ratio V <sub>DD</sub> = 2.5 V to 5.5 V		-85	-60	dB
V <sub>IC</sub>	Common mode input range V <sub>DD</sub> = 2.5 V to 5.5 V	0.5		V <sub>DD</sub> - 0.8	V
CMRR	Common mode rejection ratio V <sub>DD</sub> = 5.5 V, V <sub>IC</sub> = 0.5 V to 4.7 V V <sub>DD</sub> = 2.5 V, V <sub>IC</sub> = 0.5 V to 1.7 V		-63	-40	dB
Low-output swing	R <sub>L</sub> = 4 Ω, V <sub>IN+</sub> = V <sub>DD</sub> , V <sub>IN-</sub> = 0 V, Gain = 1 V/V, V <sub>IN-</sub> = 0 V or V <sub>IN+</sub> = V <sub>DD</sub>	V <sub>DD</sub> = 5.5 V	0.45		V
		V <sub>DD</sub> = 3.6 V	0.37		
		V <sub>DD</sub> = 2.5 V	0.26	0.4	
High-output swing	R <sub>L</sub> = 4 Ω, V <sub>IN+</sub> = V <sub>DD</sub> , V <sub>IN-</sub> = V <sub>DD</sub> , Gain = 1 V/V, V <sub>IN-</sub> = 0 V or V <sub>IN+</sub> = 0 V	V <sub>DD</sub> = 5.5 V	4.95		V
		V <sub>DD</sub> = 3.6 V	3.18		
		V <sub>DD</sub> = 2.5 V	2	2.13	
I <sub>IH</sub>	High-level input current, shutdown V <sub>DD</sub> = 5.5 V, V <sub>I</sub> = 5.8 V		58	100	μA
I <sub>IL</sub>	Low-level input current, shutdown V <sub>DD</sub> = 5.5 V, V <sub>I</sub> = -0.3 V		3	100	μA
I <sub>Q</sub>	Quiescent current V <sub>DD</sub> = 2.5 V to 5.5 V, no load		4	5	mA
I <sub>(SD)</sub>	Supply current V <sub>SHUTDOWN</sub> ≤ 0.5 V, V <sub>DD</sub> = 2.5 V to 5.5 V, R <sub>L</sub> = 4 Ω		0.01	1	μA
Gain	R <sub>L</sub> = 4 Ω	$\frac{38 \text{ k}\Omega}{R_1}$	$\frac{40 \text{ k}\Omega}{R_1}$	$\frac{42 \text{ k}\Omega}{R_1}$	V/V
Resistance from shutdown to GND			100		kΩ



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**6.6 Operating Characteristics**

T<sub>A</sub> = 25°C, Gain = 1 V/V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
P <sub>O</sub> Output power	THD + N = 1%, f = 1 kHz, R <sub>L</sub> = 3 Ω	V <sub>DD</sub> = 5 V		2.45		W
		V <sub>DD</sub> = 3.6 V		1.22		
		V <sub>DD</sub> = 2.5 V		0.49		
	THD + N = 1%, f = 1 kHz, R <sub>L</sub> = 4 Ω	V <sub>DD</sub> = 5 V		2.22		
		V <sub>DD</sub> = 3.6 V		1.1		
		V <sub>DD</sub> = 2.5 V		0.47		
	THD + N = 1%, f = 1 kHz, R <sub>L</sub> = 8 Ω	V <sub>DD</sub> = 5 V		1.36		
		V <sub>DD</sub> = 3.6 V		0.72		
		V <sub>DD</sub> = 2.5 V		0.33		
THD+N Total harmonic distortion plus noise	f = 1 kHz, R <sub>L</sub> = 3 Ω	P <sub>O</sub> = 2 W, V <sub>DD</sub> = 5 V		0.045%		
		P <sub>O</sub> = 1 W, V <sub>DD</sub> = 3.6 V		0.05%		
		P <sub>O</sub> = 300 mW, V <sub>DD</sub> = 2.5 V		0.06%		
	f = 1 kHz, R <sub>L</sub> = 4 Ω	P <sub>O</sub> = 1.8 W, V <sub>DD</sub> = 5 V		0.03%		
		P <sub>O</sub> = 0.7 W, V <sub>DD</sub> = 3.6 V		0.03%		
		P <sub>O</sub> = 300 mW, V <sub>DD</sub> = 2.5 V		0.04%		
	f = 1 kHz, R <sub>L</sub> = 8 Ω	P <sub>O</sub> = 1 W, V <sub>DD</sub> = 5 V		0.02%		
		P <sub>O</sub> = 0.5 W, V <sub>DD</sub> = 3.6 V		0.02%		
		P <sub>O</sub> = 200 mW, V <sub>DD</sub> = 2.5 V		0.03%		
k <sub>SVR</sub> Supply ripple rejection ratio	V <sub>DD</sub> = 3.6 V, Inputs AC-grounded with C <sub>I</sub> = 2 μF, V <sub>RIPPLE</sub> = 200 mV <sub>pp</sub>	f = 217 Hz		-80		dB
		f = 20 Hz to 20 kHz		-70		
SNR Signal-to-noise ratio	V <sub>DD</sub> = 5 V, P <sub>O</sub> = 2 W, R <sub>L</sub> = 4 Ω			105		dB
V <sub>n</sub> Output voltage noise	V <sub>DD</sub> = 3.6 V, f = 20 Hz to 20 kHz, Inputs AC-grounded with C <sub>I</sub> = 2 μF	No weighting		15		μV <sub>RMS</sub>
		A weighting		12		
CMRR Common mode rejection ratio	V <sub>DD</sub> = 3.6 V, V <sub>IC</sub> = 1 V <sub>pp</sub>	f = 217 Hz		-65		dB
Z <sub>I</sub> Input impedance			38	40	44	kΩ
Start-up time from shutdown	V <sub>DD</sub> = 3.6 V, No C <sub>BYPASS</sub>			4		μs
	V <sub>DD</sub> = 3.6 V, C <sub>BYPASS</sub> = 0.1 μF			27		ms

**6.7 Dissipation Ratings**

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR <sup>(1)</sup>	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DGN	2.13 W	17.1 mW/°C	1.36 W	1.11 W

(1) Derating factor based on High-k board layout.

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[www.ti.com](http://www.ti.com)**6.8 Typical Characteristics****Table 1. Table of Graphs**

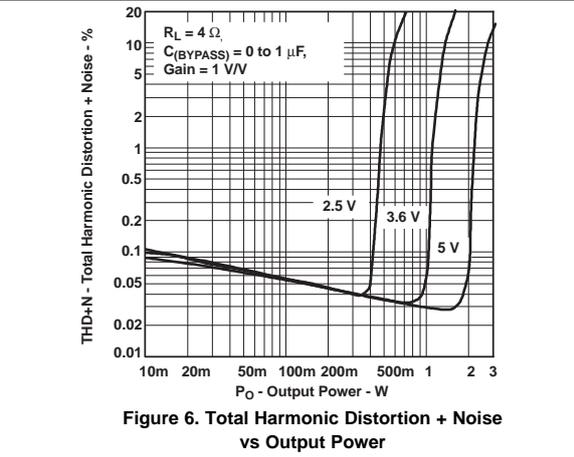
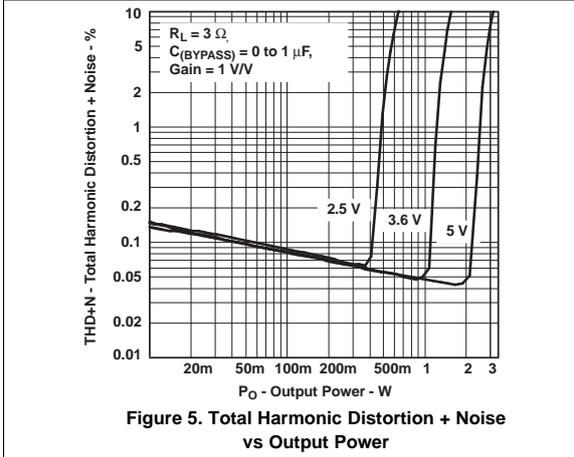
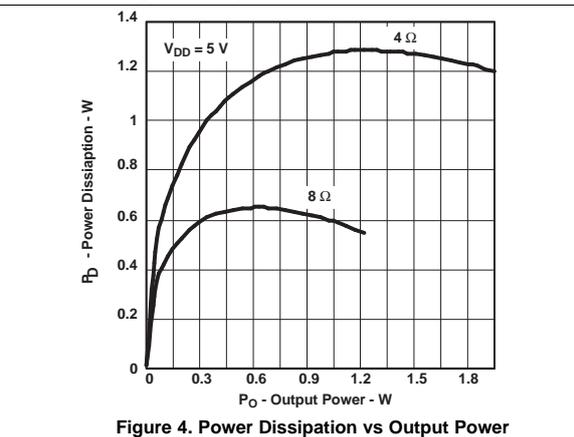
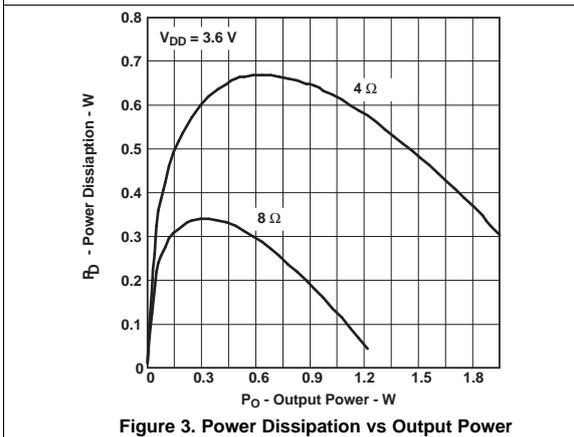
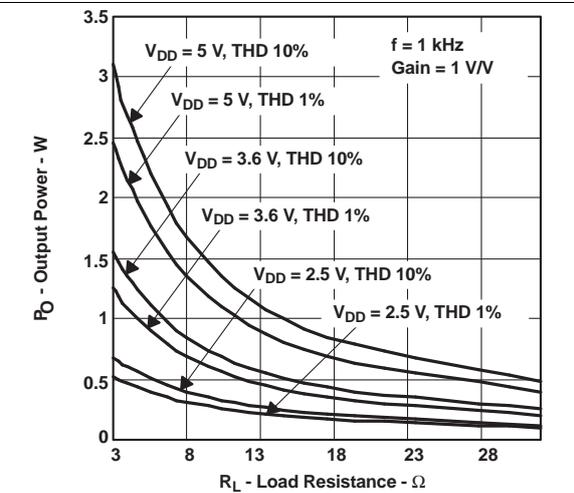
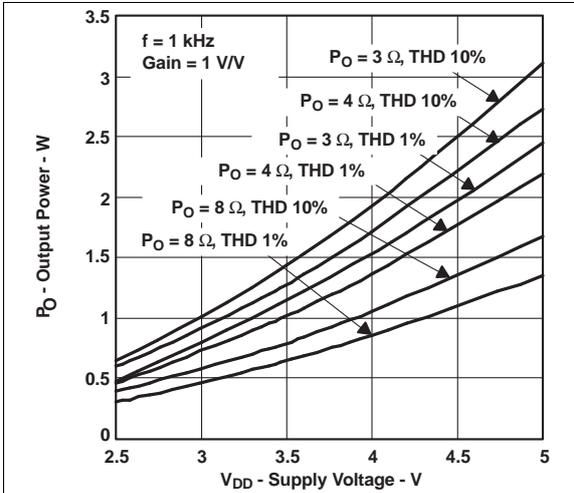
		<b>FIGURE</b>
Output power	vs Supply voltage	<a href="#">Figure 1</a>
	vs Load resistance	<a href="#">Figure 2</a>
Power dissipation	vs Output power	<a href="#">Figure 3</a> , <a href="#">Figure 4</a>
Total harmonic distortion + noise	vs Output power	<a href="#">Figure 5</a> , <a href="#">Figure 6</a> , <a href="#">Figure 7</a>
	vs Frequency	<a href="#">Figure 8</a> , <a href="#">Figure 9</a> , <a href="#">Figure 10</a> , <a href="#">Figure 11</a> , <a href="#">Figure 12</a>
	vs Common-mode input voltage	<a href="#">Figure 13</a>
Supply voltage rejection ratio	vs Frequency	<a href="#">Figure 14</a> , <a href="#">Figure 15</a> , <a href="#">Figure 16</a> , <a href="#">Figure 17</a>
Supply voltage rejection ratio	vs Common-mode input voltage	<a href="#">Figure 18</a>
GSM Power supply rejection	vs Time	<a href="#">Figure 19</a>
GSM Power supply rejection	vs Frequency	<a href="#">Figure 20</a>
Common-mode rejection ratio	vs Frequency	<a href="#">Figure 21</a>
	vs Common-mode input voltage	<a href="#">Figure 22</a>
Closed loop gain/phase	vs Frequency	<a href="#">Figure 23</a>
Open loop gain/phase	vs Frequency	<a href="#">Figure 24</a>
Supply current	vs Supply voltage	<a href="#">Figure 25</a>
	vs Shutdown voltage	<a href="#">Figure 26</a>
Start-up time	vs Bypass capacitor	<a href="#">Figure 27</a>



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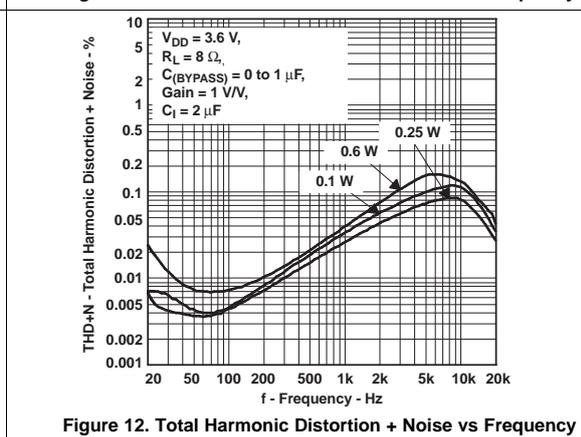
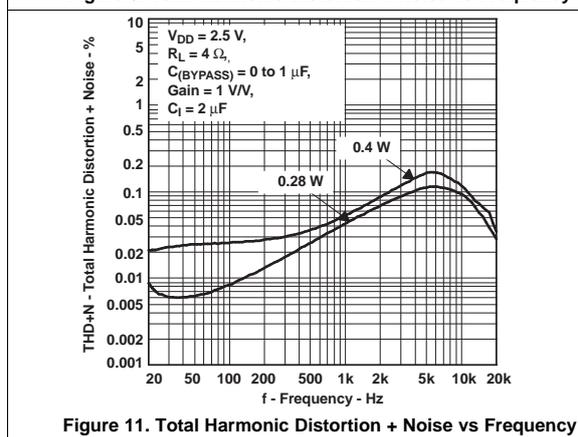
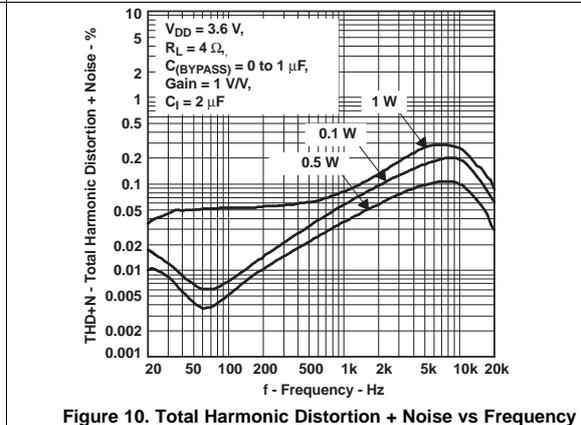
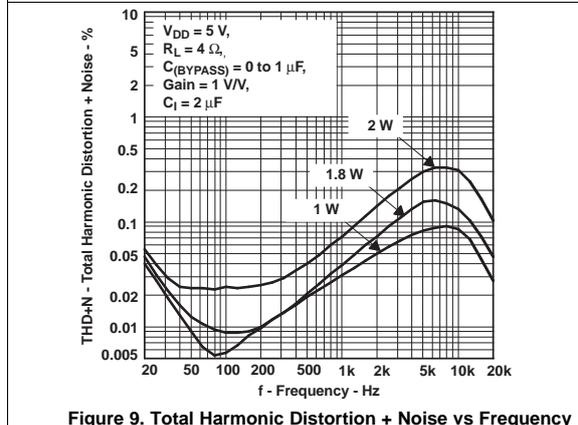
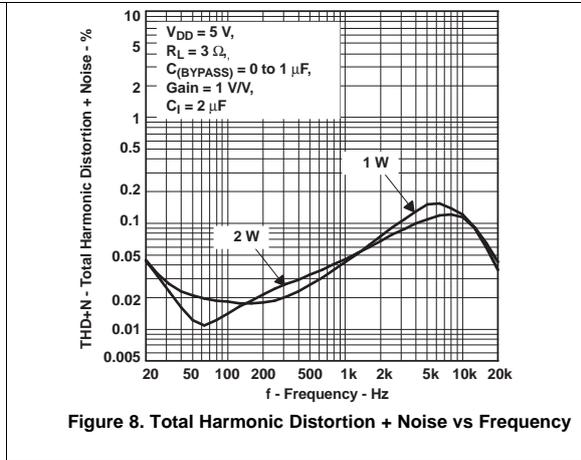
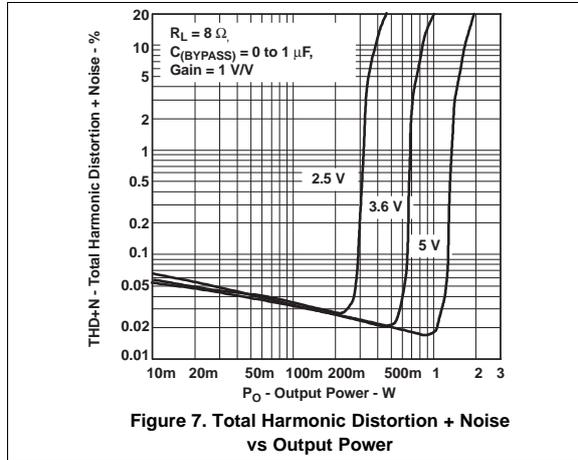




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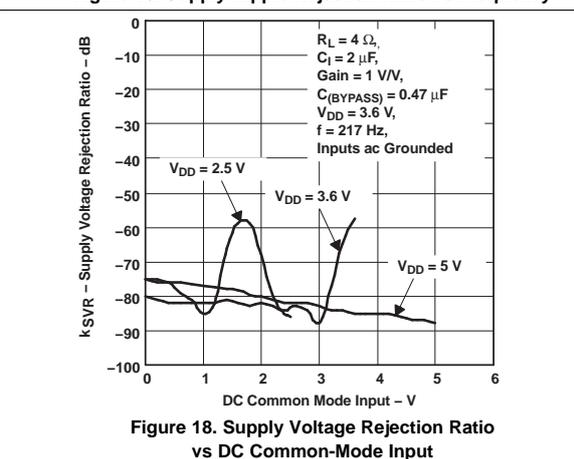
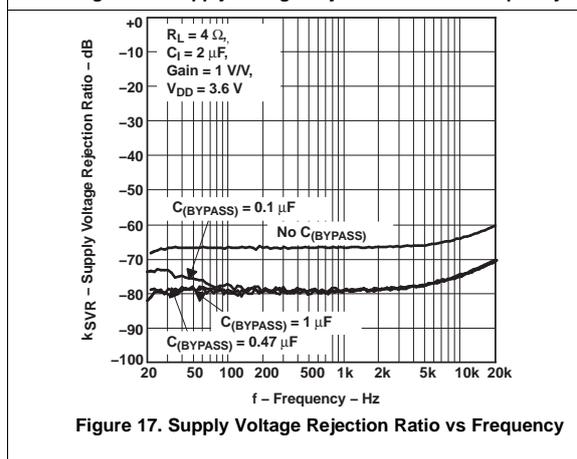
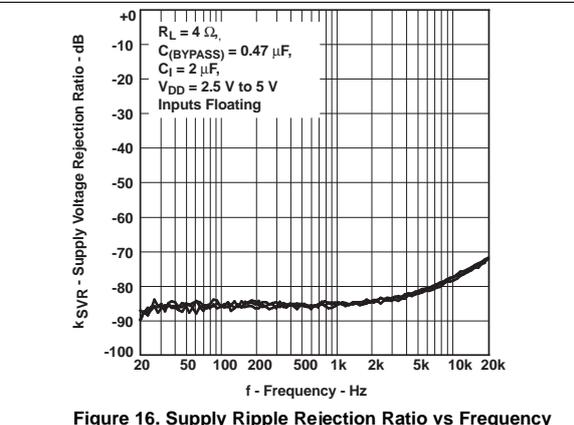
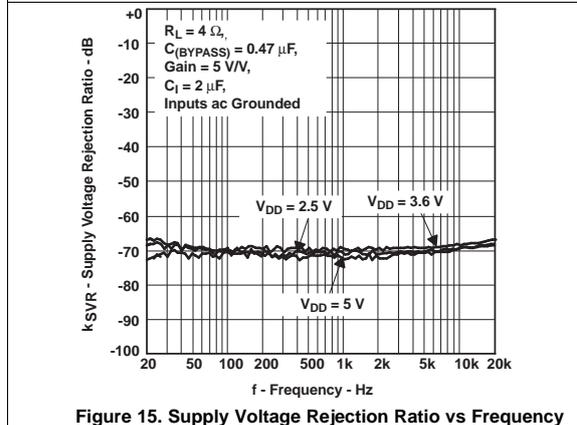
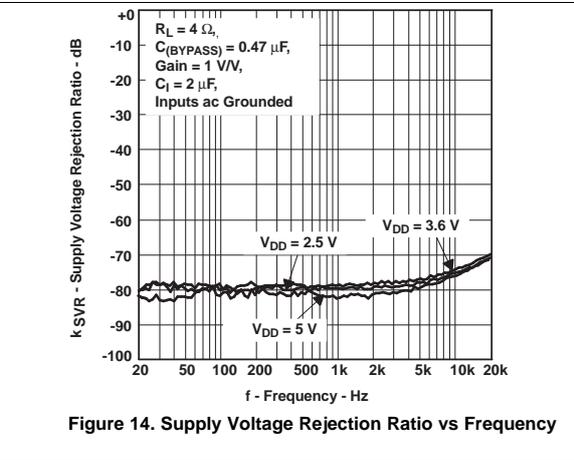
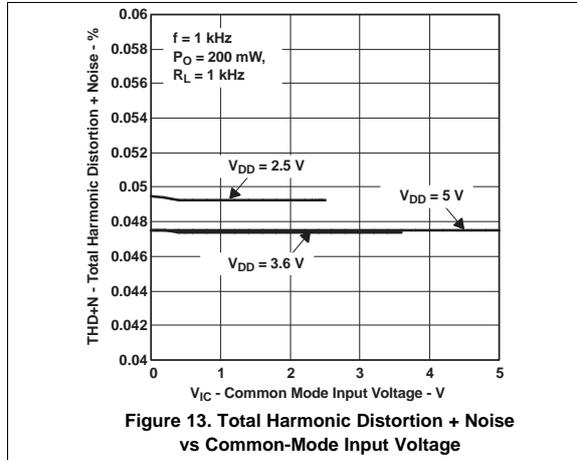




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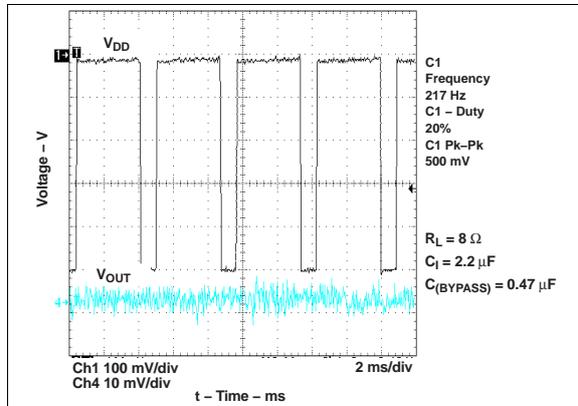


Figure 19. GSM Power Supply Rejection vs Time

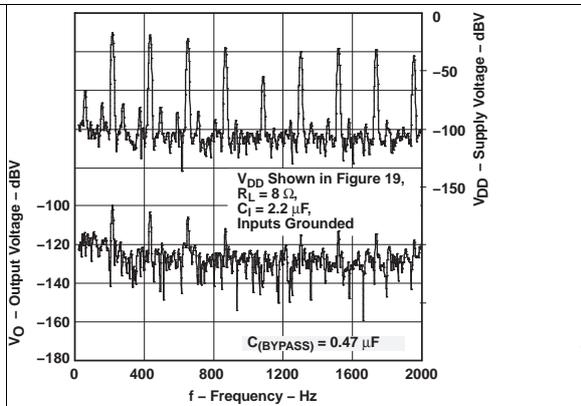


Figure 20. GSM Power Supply Rejection vs Frequency

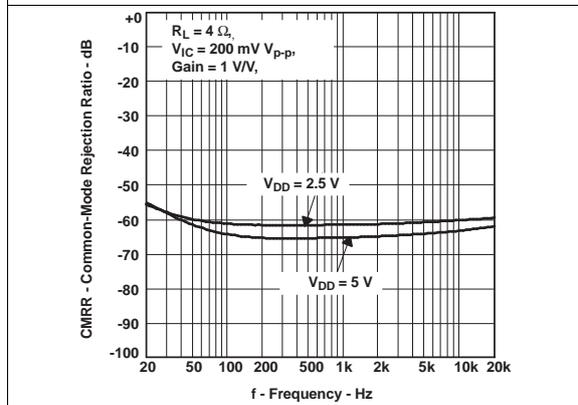


Figure 21. Common-Mode Rejection Ratio vs Frequency

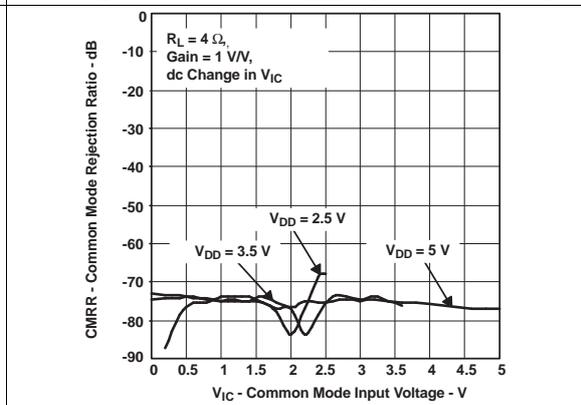


Figure 22. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

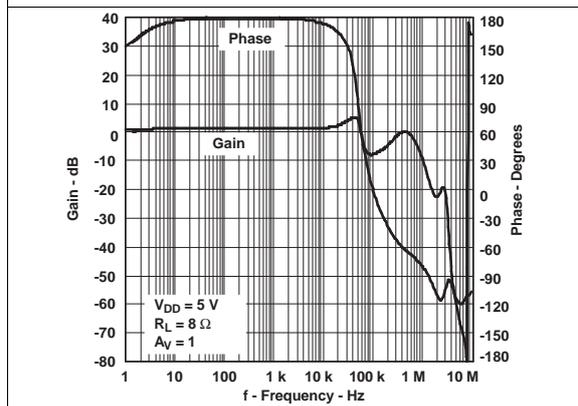


Figure 23. Closed Loop Gain/Phase vs Frequency

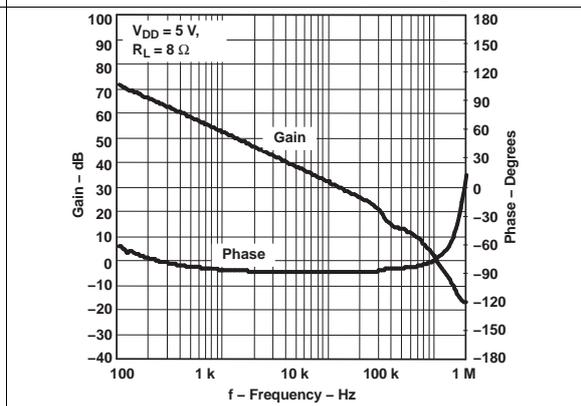


Figure 24. Open Loop Gain/Phase vs Frequency



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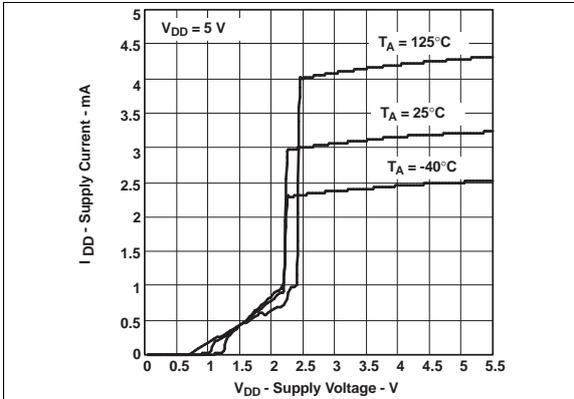


Figure 25. Supply Current vs Supply Voltage

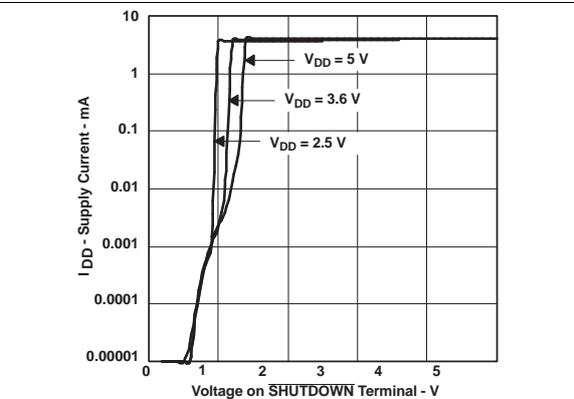


Figure 26. Supply Current vs Shutdown Voltage

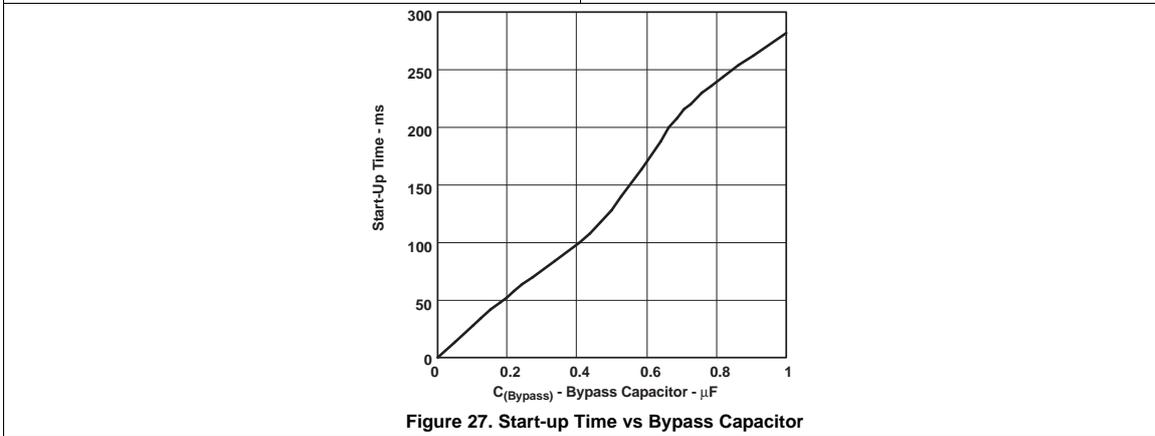


Figure 27. Start-up Time vs Bypass Capacitor



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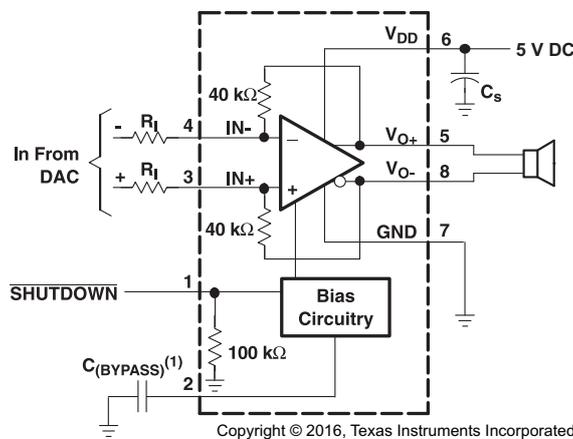
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**7 Detailed Description**

**7.1 Overview**

The TPA6211A1-Q1 device is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around  $V_{DD} / 2$  regardless of the common-mode voltage at the input.

**7.2 Functional Block Diagram**



(1)  $C_{(BYPASS)}$  is optional

**7.3 Feature Description**

**7.3.1 Advantages of Fully Differential Amplifiers**

Input coupling capacitors are not required. A fully differential amplifier with good CMRR, such as the TPA6211A1-Q1 device, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has a lower mid-supply voltage than that of the TPA6211A1-Q1 device, the common-mode feedback circuit compensates, and the outputs are still biased at the mid-supply point of the TPA6211A1-Q1 device. The inputs of the TPA6211A1-Q1 device can be biased from 0.5 V to  $V_{DD} - 0.8$  V. If the inputs are biased outside of that range, input coupling capacitors are required.

A Mid-supply bypass capacitor,  $C_{BYPASS}$ , is not required. The fully differential amplifier does not require a bypass capacitor. Any shift in the mid-supply voltage affects both positive and negative channels equally, thus canceling at the differential output. Removing the bypass capacitor slightly worsens power supply rejection ratio ( $k_{SVR}$ ), but a slight decrease of  $k_{SVR}$  can be acceptable when an additional component can be eliminated (see Figure 17).

The RF-immunity is improved. A fully differential amplifier cancels the noise from RF disturbances much better than the typical audio amplifier.

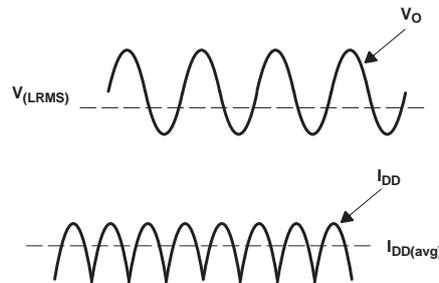
**7.3.2 Fully Differential Amplifier Efficiency and Thermal Information**

Class-AB amplifiers are inefficient, primarily because of voltage drop across the output-stage transistors. The two components of this internal voltage drop are the headroom or DC voltage drop that varies inversely to output power, and the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from  $V_{DD}$ . The internal voltage drop multiplied by the average value of the supply current,  $I_{DD}(avg)$ , determines the internal power dissipation of the amplifier.



**Feature Description (continued)**

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see [Figure 28](#)).



**Figure 28. Voltage and Current Waveforms for BTL Amplifiers**

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL the current waveform is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. [Equation 1](#) to [Equation 10](#) are the basis for calculating amplifier efficiency.

$$\eta_{BTL} = \frac{P_L}{P_{SUP}}$$

where

- $\eta_{BTL}$  is the efficiency of a BTL amplifier
- $P_L$  is the power delivered to load
- $P_{SUP}$  is the power drawn from power supply

(1)

$P_L$  is calculated with [Equation 2](#), and  $V_{LRMS}$  is calculated with [Equation 3](#).

$$P_L = \frac{V_{LRMS}^2}{R_L}$$

where

- $V_{LRMS}$  = RMS voltage on BTL load
- $R_L$  is load resistance

(2)

$$V_{LRMS} = \frac{V_P}{\sqrt{2}}$$

where

- $V_P$  is peak voltage on BTL load

(3)

Therefore,  $P_L$  can be given as [Equation 4](#).

$$P_L = \frac{V_P^2}{2 \times R_L}$$

(4)

$P_{SUP}$  is calculated with [Equation 5](#).

$$P_{SUP} = V_{DD} \times I_{DDavg}$$

where

- $V_{DD}$  is power supply voltage
- $I_{DDavg}$  is average current drawn from the power supply

(5)



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**Feature Description (continued)**

$I_{DDavg}$  is calculated with Equation 6.

$$I_{DDavg} = \frac{1}{\pi} \int_0^{\pi} \frac{V_P}{R_L} \times \sin(t) \times dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} \times \cos(t) \Big|_0^{\pi} = \frac{2 \times V_P}{\pi \times R_L} \tag{6}$$

Therefore,  $P_{SUP}$  can be given as Equation 7.

$$P_{SUP} = \frac{2 \times V_{DD} \times V_P}{\pi \times R_L} \tag{7}$$

Substituting for  $P_L$  and  $P_{SUP}$ , Equation 1 becomes Equation 8

$$\eta_{BTL} = \frac{\frac{V_P^2}{2 \times R_L}}{\frac{2 \times V_{DD} \times V_P}{\pi \times R_L}} = \frac{\pi \times V_P}{4 \times V_{DD}} \tag{8}$$

$V_P$  is calculated with Equation 9.

$$V_P = \sqrt{2 \times P_L \times R_L} \tag{9}$$

And substituting for  $V_P$ ,  $\eta_{BTL}$  can be calculated with Equation 10

$$\eta_{BTL} = \frac{\pi \sqrt{2 \times P_L \times R_L}}{4 \times V_{DD}} \tag{10}$$

A simple formula for calculating the maximum power dissipated ( $P_{Dmax}$ ) can be used for a differential output application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

**Table 2. Efficiency and Maximum Ambient Temperature vs Output Power**

OUTPUT POWER	EFFICIENCY	INTERNAL DISSIPATION	POWER FROM SUPPLY	MAX AMBIENT TEMPERATURE
<b>5-V, 3-Ω SYSTEMS</b>				
0.5 W	27.2%	1.34 W	1.84 W	54°C
1 W	38.4%	1.6 W	2.6 W	35°C
2.45 W	60.2%	1.62 W	4.07 W	34°C
3.1 W	67.7%	1.48 W	4.58 W	44°C
<b>5-V, 4-Ω BTL SYSTEMS</b>				
0.5 W	31.4%	1.09 W	1.59 W	72°C
1 W	44.4%	1.25 W	2.25 W	60°C
2 W	62.8%	1.18 W	3.18 W	65°C
2.8 W	74.3%	0.97 W	3.77 W	80°C
<b>5-V, 8-Ω SYSTEMS</b>				
0.5 W	44.4%	0.625 W	1.13 W	105°C (limited by maximum ambient temperature specification)
1 W	62.8%	0.592 W	1.6 W	105°C (limited by maximum ambient temperature specification)
1.36 W	73.3%	0.496 W	1.86 W	105°C (limited by maximum ambient temperature specification)
1.7 W	81.9%	0.375 W	2.08 W	105°C (limited by maximum ambient temperature specification)



Equation 10 is used to calculate efficiencies for four different output power levels, see Table 2. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 2.8-W audio system with 4-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.8 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. In Equation 10,  $V_{DD}$  is in the denominator. This indicates that as  $V_{DD}$  goes down, efficiency goes up.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. Given  $R_{\theta JA}$  (junction-to-ambient thermal resistance), the maximum allowable junction temperature, and the internal dissipation at 1-W output power with a 4-Ohm load, the maximum ambient temperature can be calculated with Equation 12. The maximum recommended junction temperature for the TPA6211A1-Q1 device is 150°C.

$$T_A(\text{Max}) = T_J(\text{Max}) - R_{\theta JA} \times P_D = 150 - 71.7 \times 1.25 = 60^\circ\text{C} \tag{12}$$

Equation 12 shows that the maximum ambient temperature is 60°C at 1-W output power and 4-Ohm load with a 5-V supply.

Table 2 shows that the thermal performance must be considered when using a Class-AB amplifier to keep junction temperatures in the specified range. The TPA6211A1-Q1 device is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. In addition, using speakers with an impedance higher than 4 Ω dramatically increases the thermal performance by reducing the output current.

**7.3.3 Differential Output Versus Single-Ended Output**

Figure 29 shows a Class-AB audio power amplifier (APA) in a fully differential configuration. The TPA6211A1-Q1 amplifier has differential outputs driving both ends of the load. One of several potential benefits to this configuration is power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground-referenced load. Plugging  $2 \times V_{O(PP)}$  into the power equation (Equation 13) yields four-times the output power (as the voltage is squared) from the same supply rail and load impedance (see Equation 15 and Equation 16).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \tag{13}$$

$$\text{Power}_{(S-E)} = \frac{V_{(rms)}^2}{R_L} = \frac{\left(\frac{V_{O(PP)}}{2\sqrt{2}}\right)^2}{R_L} = \frac{V_{O(PP)}^2}{8R_L} \tag{14}$$

$$\text{Power}_{(Diff)} = \frac{V_{(rms)}^2}{R_L} = \frac{\left(\frac{2 \times V_{O(PP)}}{2\sqrt{2}}\right)^2}{R_L} = \frac{V_{O(PP)}^2}{2R_L} \tag{15}$$

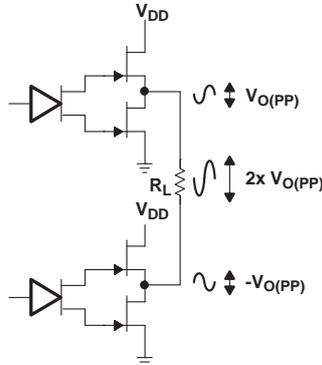
$$\text{Power}_{(Diff)} = 4 \times \text{Power}_{(S-E)} \tag{16}$$



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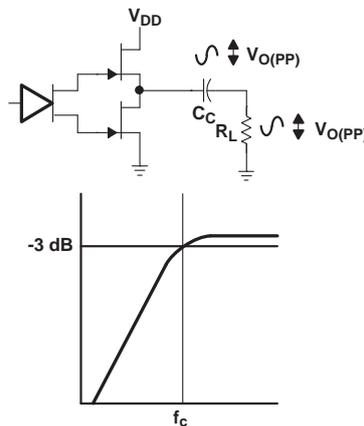


**Figure 29. Differential Output Configuration**

In a typical automotive application operating at 5 V, bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 390 mW to 1.56 W. This is a 6-dB improvement in sound power, or loudness of the sound. In addition to increased power, there are frequency-response concerns. Consider the single-supply SE configuration shown in Figure 30. A coupling capacitor (C<sub>C</sub>) is required to block the DC-offset voltage from the load. This capacitor can be quite large (approximately 33 μF to 1000 μF) so it tends to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance. This frequency-limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance. This is calculated with Equation 17.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{17}$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the DC offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.



**Figure 30. Single-Ended Output and Frequency Response**

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces four-times the output power of the SE configuration.

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#### 7.4 Device Functional Modes

The TPA6211A1-Q1 device can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to SHUTDOWN pin.



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**8 Application and Implementation**

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

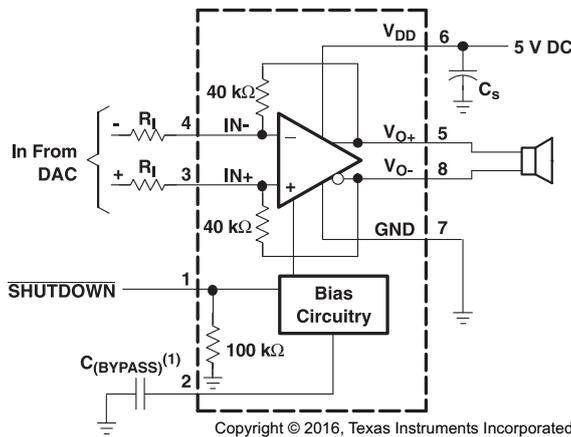
**8.1 Application Information**

The TPA6211A1-Q1 is a fully-differential amplifier designed to drive a speaker with at least 3-Ω impedance while consuming only 20-mm<sup>2</sup> total printed-circuit board (PCB) area in most applications.

**8.2 Typical Applications**

Figure 31 shows a typical application circuit for the TPA6211A1-Q1 with a speaker, input resistors, and supporting power supply decoupling capacitors.

**8.2.1 Typical Differential Input Application**



(1) C<sub>(BYPASS)</sub> is optional

**Figure 31. Typical Differential Input Application Schematic**

Typical values are shown in Table 3.

**Table 3. Typical Component Values**

COMPONENT	VALUE
R <sub>i</sub>	40 kΩ
C <sub>(BYPASS)</sub> <sup>(1)</sup>	0.22 μF
C <sub>S</sub>	1 μF
C <sub>I</sub>	0.22 μF

(1) C<sub>(BYPASS)</sub> is optional.

**8.2.1.1 Design Requirements**

For this design example, use the parameters listed in Table 4 as the input parameters.



**Table 4. Design Parameters**

PARAMETER	EXAMPLE VALUE
Power supply voltage	2.5 V to 5.5 V
Current	4 mA to 5 mA
Shutdown	High > 1.55 V
	Low < 0.5 V
Speaker	3 Ω, 4 Ω, or 8 Ω

**8.2.1.2 Detailed Design Procedure**

**8.2.1.2.1 Resistors (R<sub>I</sub>)**

The input resistor (R<sub>I</sub>) can be selected to set the gain of the amplifier according to [Equation 18](#).

$$\text{Gain} = \frac{R_F}{R_I} \tag{18}$$

The internal feedback resistors (R<sub>F</sub>) are trimmed to 40 kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, TI recommends 1%-tolerance resistors or better to optimize performance.

**8.2.1.2.2 Bypass Capacitor (C<sub>BYPASS</sub>) and Start-Up Time**

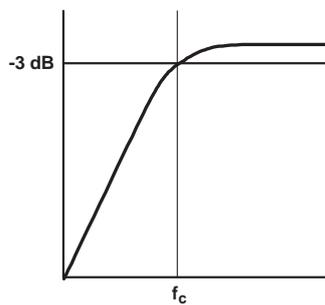
The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to V<sub>DD</sub> / 2. Adding a capacitor filters any noise into this pin, increasing k<sub>SVR</sub>. C<sub>BYPASS</sub> also determines the rise time of V<sub>O+</sub> and V<sub>O-</sub> when the device exits shutdown. The larger the capacitor, the slower the rise time.

**8.2.1.2.3 Input Capacitor (C<sub>I</sub>)**

The TPA6211A1-Q1 device does not require input coupling capacitors when driven by a differential input source biased from 0.5 V to V<sub>DD</sub> – 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application, an input capacitor (C<sub>I</sub>) is required to allow the amplifier to bias the input signal to the proper DC level. In this case, C<sub>I</sub> and R<sub>I</sub> form a high-pass filter with the corner frequency defined in [Equation 19](#).

$$f_c = \frac{1}{2\pi R_I C_I} \tag{19}$$



**Figure 32. Input Filter Cutoff Frequency**

The value of C<sub>I</sub> is an important consideration, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R<sub>I</sub> is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. [Equation 19](#) is reconfigured as [Equation 20](#).

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$$C_1 = \frac{1}{2\pi R_1 f_c} \quad (20)$$

In this example,  $C_1$  is 0.16  $\mu\text{F}$ , so the likely choice ranges from 0.22  $\mu\text{F}$  to 0.47  $\mu\text{F}$ . TI recommends the use of ceramic capacitors because they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor faces the amplifier input in most applications. The input DC level is held at  $V_{DD} / 2$ , typically higher than the source DC level. Confirming the capacitor polarity in the application is important.

**8.2.1.2.4 Band-Pass Filter ( $R_1$ ,  $C_1$ , and  $C_F$ )**

Having signal filtering beyond the one-pole high-pass filter formed by the combination of  $C_1$  and  $R_1$  can be desirable. A low-pass filter can be added by placing a capacitor ( $C_F$ ) between the inputs and outputs, forming a band-pass filter.

An example of when this technique might be used would be in an application where the desirable pass-band range is between 100 Hz and 10 kHz, with a gain of 4 V/V. Equation 21 to Equation 28 allow the proper values of  $C_F$  and  $C_1$  to be determined.

**8.2.1.2.4.1 Step 1: Low-Pass Filter**

$$f_{c(\text{LPF})} = \frac{1}{2\pi R_F C_F} \quad (21)$$

$$f_{c(\text{LPF})} = \frac{1}{2\pi 40\text{k}\Omega C_F} \quad (22)$$

Therefore,

$$C_F = \frac{1}{2\pi 40\text{k}\Omega f_{c(\text{LPF})}} \quad (23)$$

Substituting 10 kHz for  $f_{c(\text{LPF})}$  and solving for  $C_F$ :

$$C_F = 398\text{ pF} \quad (24)$$

**8.2.1.2.4.2 Step 2: High-Pass Filter**

$$f_{c(\text{HPF})} = \frac{1}{2\pi R_1 C_1} \quad (25)$$

Because the application in this case requires a gain of 4 V/V,  $R_1$  must be set to 10 k $\Omega$ .

Substituting  $R_1$  into Equation 25.

$$f_{c(\text{HPF})} = \frac{1}{2\pi 10\text{ k}\Omega C_1} \quad (26)$$

Therefore,

$$C_1 = \frac{1}{2\pi 10\text{ k}\Omega f_{c(\text{HPF})}} \quad (27)$$

Substituting 100 Hz for  $f_{c(\text{HPF})}$  and solving for  $C_1$ :

$$C_1 = 0.16\text{ }\mu\text{F} \quad (28)$$

At this point, a first-order band-pass filter has been created with the low-frequency cutoff set to 100 Hz and the high-frequency cutoff set to 10 kHz.

The process can be taken a step further by creating a second-order high-pass filter. This is accomplished by placing a resistor ( $R_a$ ) and capacitor ( $C_a$ ) in the input path.  $R_a$  must be at least 10 times smaller than  $R_1$ ; otherwise its value has a noticeable effect on the gain, as  $R_a$  and  $R_1$  are in series.

**8.2.1.2.4.3 Step 3: Additional Low-Pass Filter**

$R_a$  must be at least ten-times smaller than  $R_1$ . Set  $R_a = 1\text{ k}\Omega$



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$$f_{c(LPF)} = \frac{1}{2\pi R_a C_a} \tag{29}$$

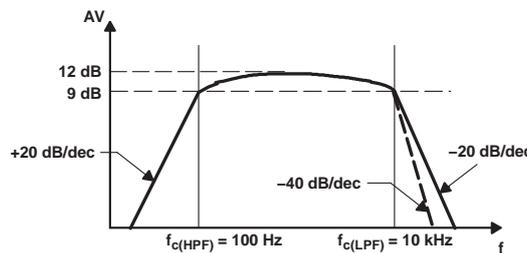
Therefore,

$$C_a = \frac{1}{2\pi \cdot 1k\Omega \cdot f_{c(LPF)}} \tag{30}$$

Substituting 10 kHz for  $f_{c(LPF)}$  and solving for  $C_a$ :

$$C_a = 160 \text{ pF} \tag{31}$$

Figure 33 is a bode plot for the band-pass filter in the previous example. Figure 38 shows how to configure the TPA6211A1-Q1 device as a band-pass filter.



**Figure 33. Bode Plot**

**8.2.1.2.5 Decoupling Capacitor ( $C_s$ )**

The TPA6211A1-Q1 device is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$ , placed as close as possible to the device  $V_{DD}$  lead works best. For filtering lower frequency noise signals, a 10- $\mu\text{F}$  or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

**8.2.1.2.6 Using Low-ESR Capacitors**

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

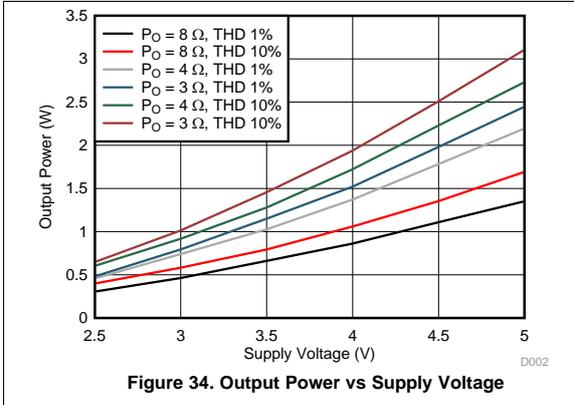


**TPA6211A1-Q1**

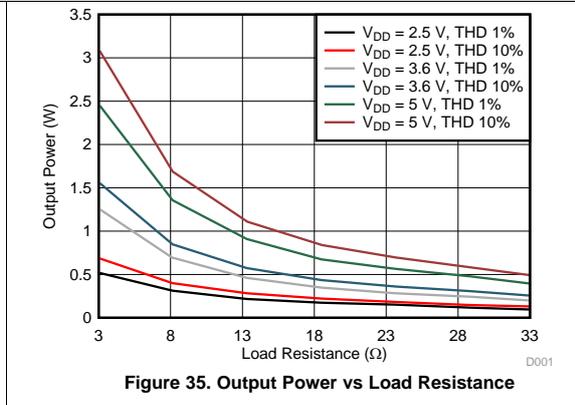
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**8.2.1.3 Application Curves**



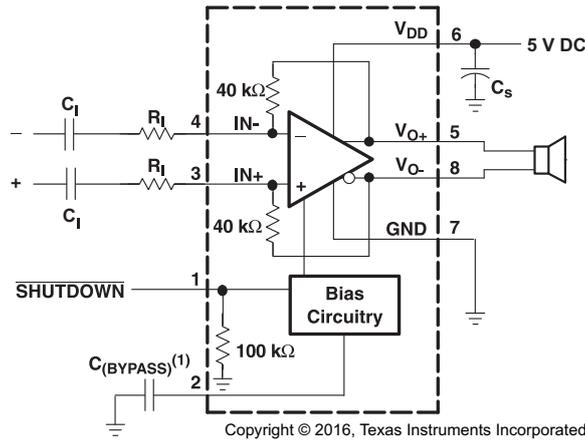
**Figure 34. Output Power vs Supply Voltage**



**Figure 35. Output Power vs Load Resistance**

**8.2.2 Other Application Circuits**

Figure 36, Figure 37, and Figure 38 show example circuits using the TPA6211A1-Q1 device.



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(1)  $C_{(BYPASS)}$  is optional

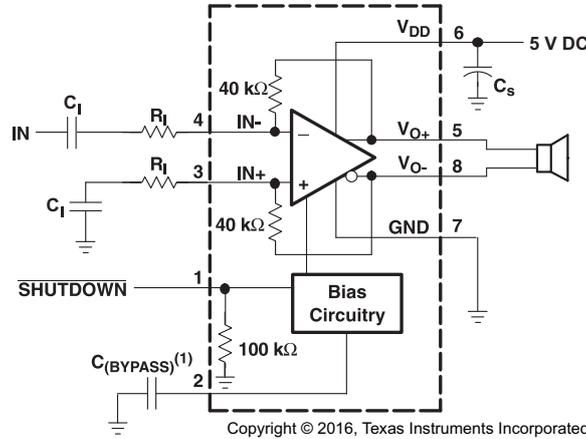
**Figure 36. Differential Input Application Schematic Optimized With Input Capacitors**



**TPA6211A1-Q1**

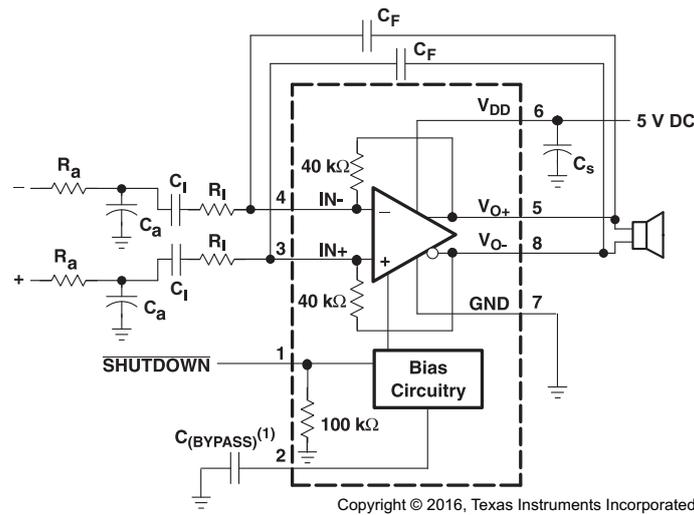
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(1) C<sub>(BYPASS)</sub> is optional

**Figure 37. Single-Ended Input Application Schematic**



(1) C<sub>(BYPASS)</sub> is optional

**Figure 38. Differential Input Application Schematic With Input Bandpass Filter**

**9 Power Supply Recommendations**

The TPA6211A1-Q1 device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. Therefore, the output voltage range of power supply must be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.



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**9.1 Power Supply Decoupling Capacitor**

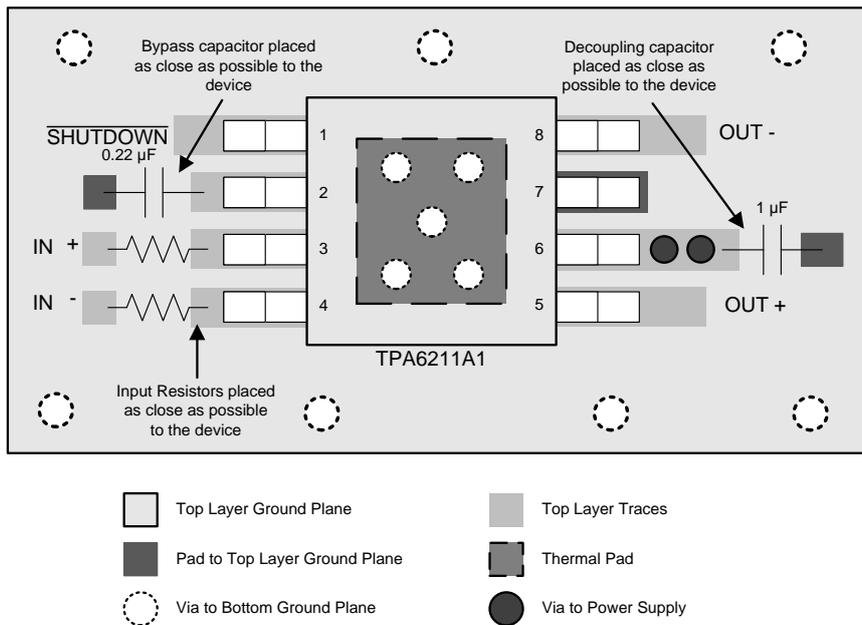
The TPA6211A1-Q1 device requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent series resistance (ESR) ceramic capacitor, typically 0.1  $\mu\text{F}$ , as close as possible of the  $V_{\text{DD}}$  pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. TI recommends placing a 2.2- $\mu\text{F}$  to 10- $\mu\text{F}$  capacitor on the  $V_{\text{DD}}$  supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

**10 Layout**

**10.1 Layout Guidelines**

Place all the external components close to the TPA6211A1-Q1 device. The input resistors need to be close to the device input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the device. Placing the decoupling capacitors,  $C_{\text{S}}$  and  $C_{\text{BYPASS}}$ , close to the TPA6211A1-Q1 device is important for the efficiency of the amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

**10.2 Layout Example**



**Figure 39. TPA6211A1-Q1 8-Pin MSOP-PowerPAD™ (DGN) Board Layout**



## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.